TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS045C – Revised October 2003

CD4048B Types

CMOS Multifunction Expandable 8-Input Gate

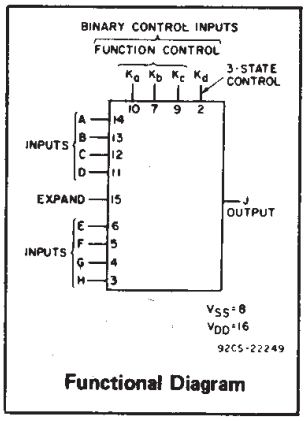
High-Voltage Types (20-Volt Rating)

■ CD4048B is an 8-input gate having four control inputs. Three binary control inputs — Ka, Kb, and Kc — provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR.

A fourth control input, Kd, provides the user with a 3-state output. When control input Kd is high, the output is either a logic 1 or a logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs into a CD4048B (see Fig. 2). For example, two CD4048Bs can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

The CD4048B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).



Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

Features:

- Three-state output
- Many logic functions available in one package
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V (full package-temperature range), 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at V_{DD}=5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD}=15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Selection of up to 8 logic functions
- Digital control of logic
- General-purpose gating logic
  - Decoding
  - Encoding

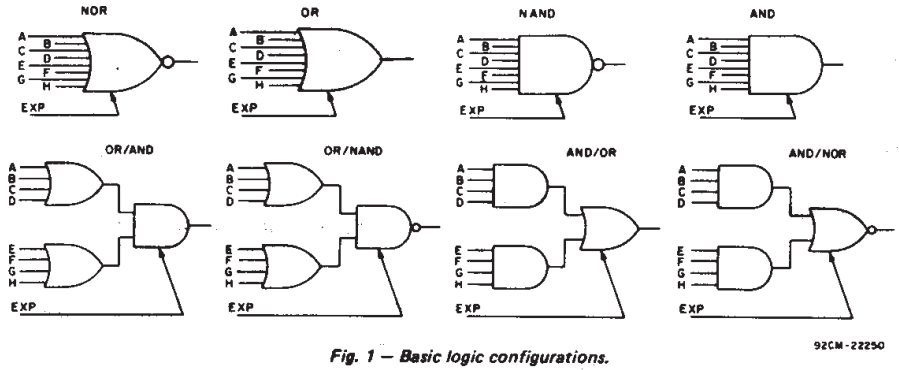
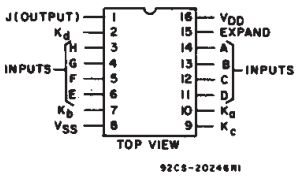


Fig. 1 — Basic logic configurations.



TERMINAL ASSIGNMENT

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

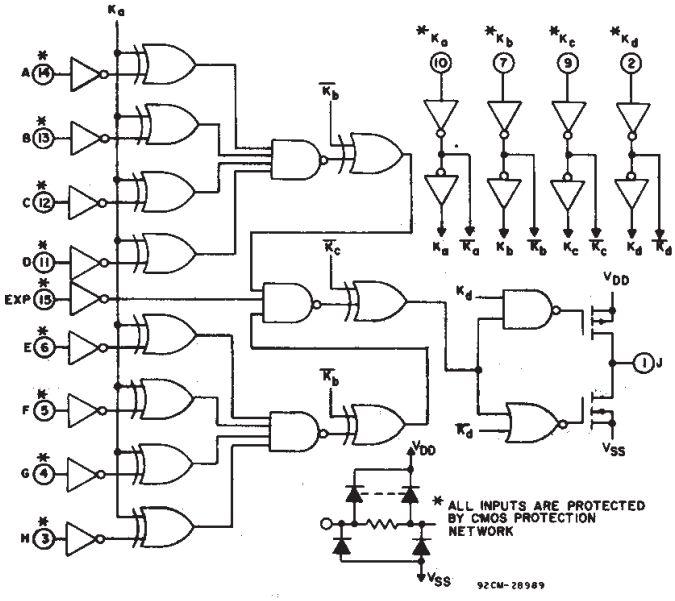


Fig. 2 – Logic diagram.

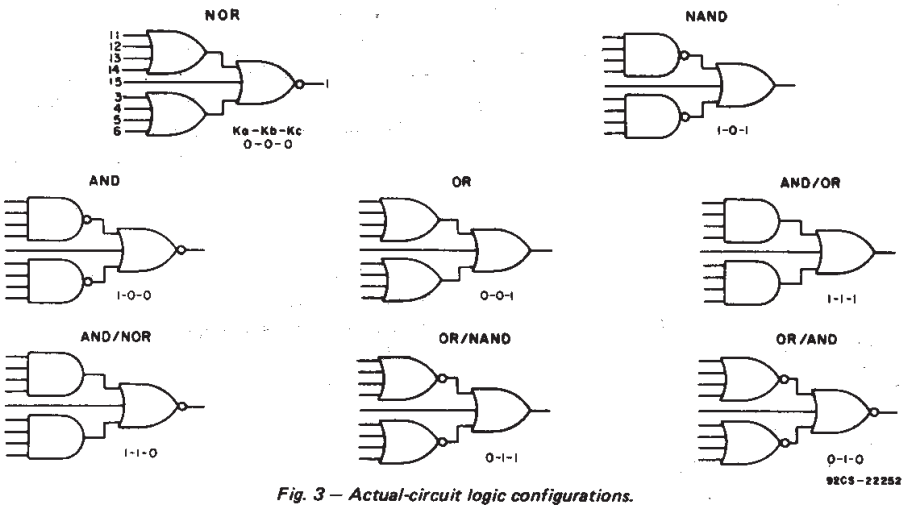


Fig. 3 – Actual-circuit logic configurations.

APPLICATIONS OF EXPAND INPUT

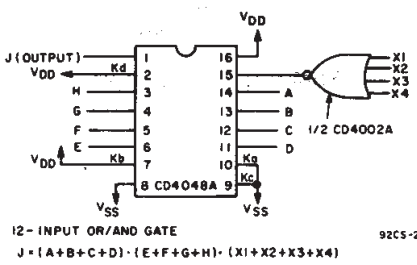


Fig. 4 – 12-input OR/AND gate.

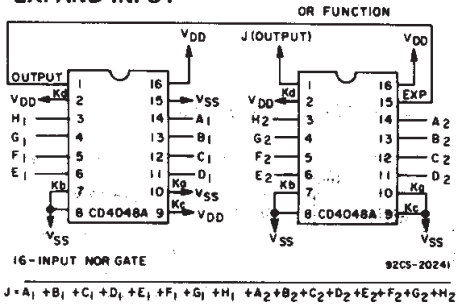


Fig. 5 – 16-input NOR gate.

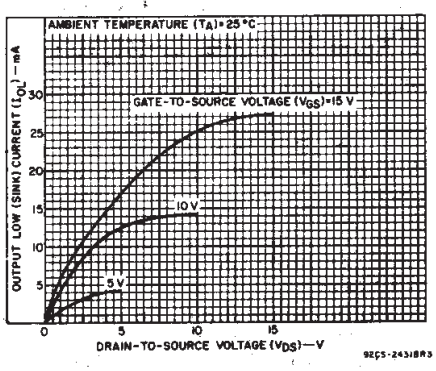


Fig. 6 – Typical output low (sink) current characteristics.

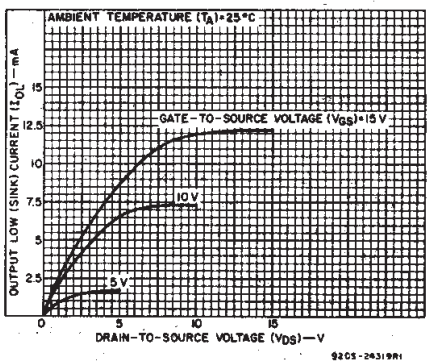


Fig. 7 – Minimum output low (sink) current characteristics.

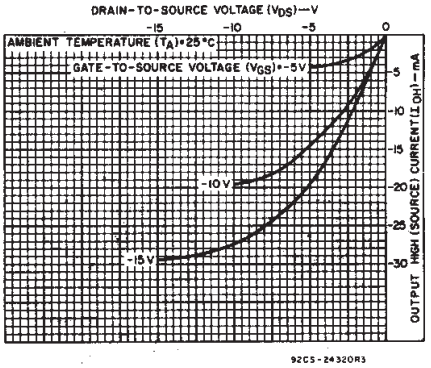


Fig. 8 – Typical output high (source) current characteristics.

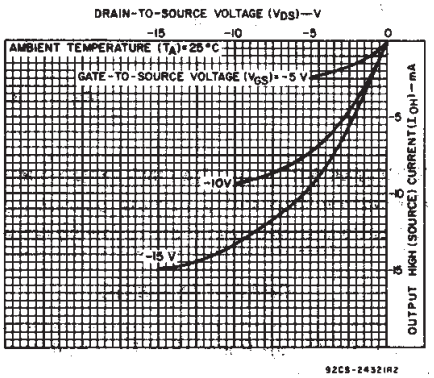


Fig. 9 – Minimum output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				—	—	1.5	V
	1,9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	—	—	
	1,9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Current, I_{OUT}	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

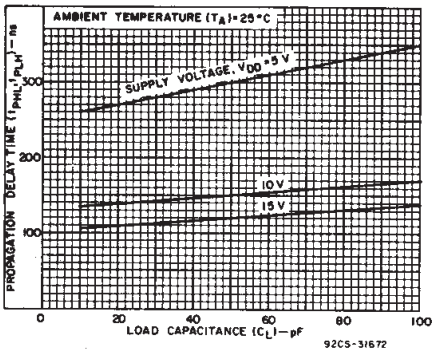


Fig. 10 – Typical propagation delay time (logic inputs to output) as a function of load capacitance.

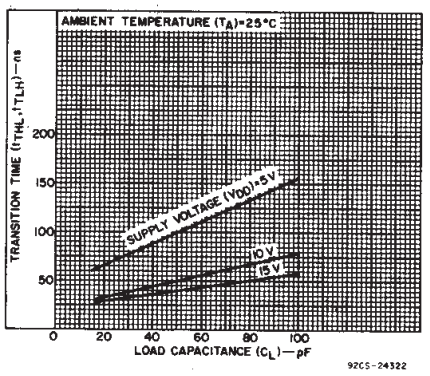


Fig. 11 – Typical transition time vs. load capacitance.

IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J=\overline{(A+B+C+D+E+F+G+H)+(EXP)}$
OR	OR	$J=(A+B+C+D+E+F+G+H)+(EXP)$
AND	NAND	$J=(ABCDEFGH)\cdot\overline{(EXP)}$
NAND	NAND	$J=\overline{(ABCDEFGH)\cdot\overline{(EXP)}}$
OR/AND	NOR	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)\cdot\overline{(EXP)}}$
OR/NAND	NOR	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)\cdot\overline{(EXP)}}$
AND/NOR	AND	$J=\overline{(ABCD)+(EFGH)+(EXP)}$
AND/OR	AND	$J=(ABCD)+(EFGH)+(EXP)$

Note: (EXP) designates the EXPAND function (i.e., $X_1+X_2+\ldots X_N$).

NOTE:
Refer to FUNCTION TRUTH TABLE for connection of unused inputs.

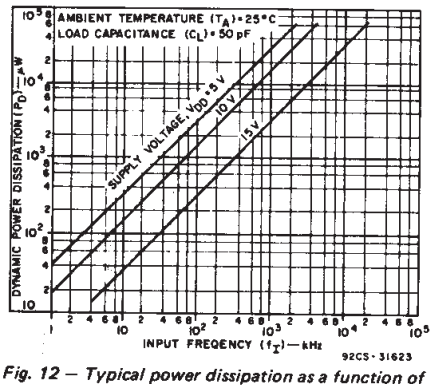


Fig. 12 – Typical power dissipation as a function of input frequency.

DYNAMIC CHARACTERISTICS at T_A=25°C, C_L=50 pF, Input t_r,t_f=20 ns, R_L=200 kΩ unless otherwise specified

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS All Package Types Typ.	LIMITS All Package Types Max.	UNITS
Propagation Delay: t_{PHL},t_{PLH} Inputs to Output and Ka to Output		5	300	600	ns
		10	150	300	
		15	120	240	
Kb to Output		5	225	450	
		10	85	170	
		15	55	110	
Kc to Output		5	140	280	
		10	50	100	
		15	40	80	
Expand Input to Output		5	190	380	
		10	90	180	
		15	65	130	
3-State Propagation Delay: Kd to Output t_{PHZ},t_{PLZ} t_{PZH},t_{PZL}	R_L=1 kΩ See Fig.21	5	80	160	
		10	35	70	
		15	25	50	
Transition Time: t_{THL},t_{TLH}		5	100	200	
		10	50	100	
		15	40	80	
Input Capacitance: C_I	Any Input		5	7	pF
3-State Output Capacitance			5	10	

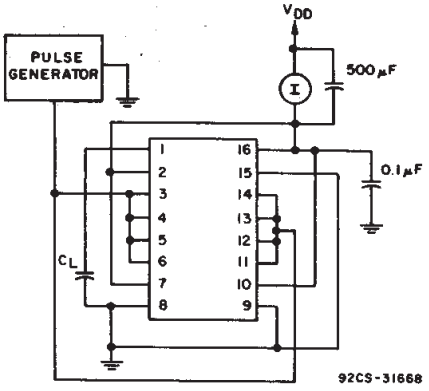


Fig. 13 – Dynamic power dissipation test circuit.

FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_a	K_b	K_c	UNUSED INPUT*
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	J=A+B+C+D+E+F+G+H	0	0	1	V_{SS}
OR/AND	J=(A+B+C+D)·(E+F+G+H)	0	1	0	V_{SS}
OR/NAND	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	J=ABCDEFGH	1	0	0	V_{DD}
NAND	$J=\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	J=ABCD+EFGH	1	1	1	V_{DD}

K_d=1 Normal Inverter Action

K_d=0 High Impedance Output

EXPAND Input=0

* See Figs. 1,2,3,4, and 5.

TEST CIRCUITS - STATIC MEASUREMENTS

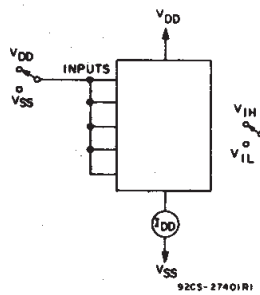


Fig. 14 – Quiescent device current test circuit.

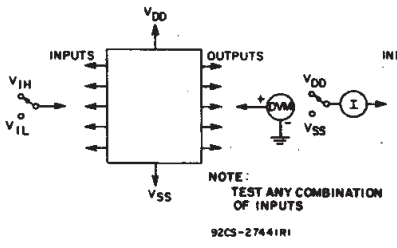


Fig. 15 – Input voltage test circuit.

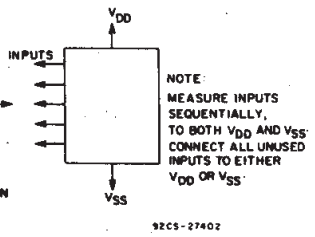


Fig. 16 – Input current test circuit.

TEST CIRCUITS - DYNAMIC MEASUREMENTS

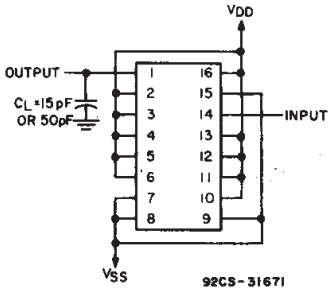


Fig. 17 – Test circuit for t_{PHL}, t_{THL}, and t_{TLH} (AND) measurements.

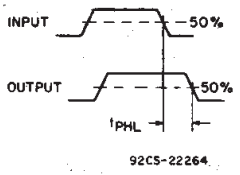


Fig. 18 – Waveforms for t_{PHL} and t_{PHL} (AND).

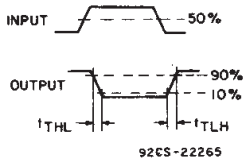


Fig. 19 – Waveforms for t_{THL} and t_{TLH} (AND).

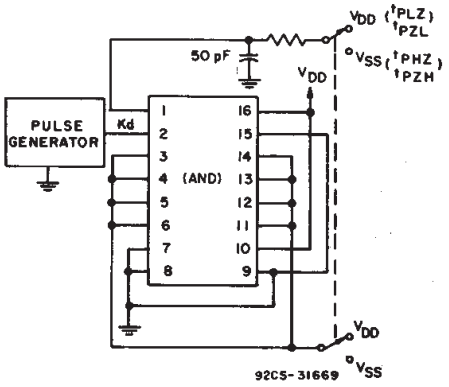


Fig. 20 – Test circuit for t_{PZL}, t_{PZH}, t_{PLZ}, and t_{PHZ} (AND).

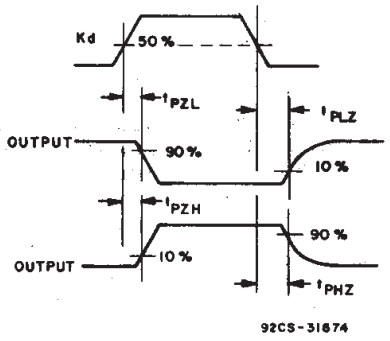
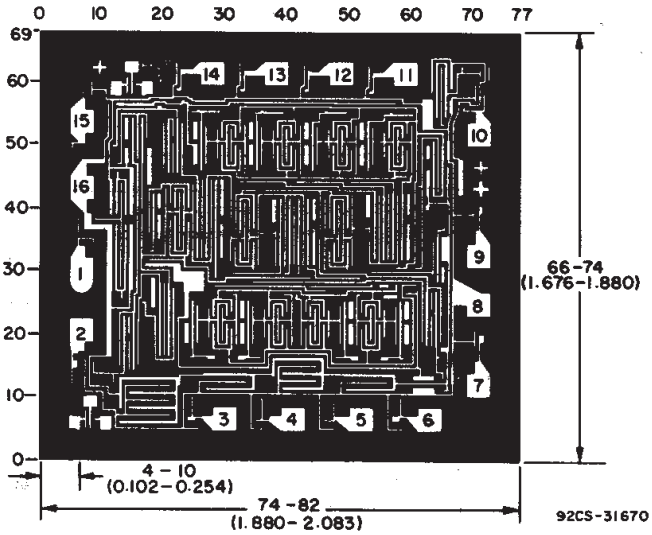


Fig. 21 – Waveforms for t_{PZL}, t_{PZH}, t_{PLZ}, and t_{PHZ} (AND).



Dimensions and pad layout for CD4048BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD4048BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4048BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4048BM	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4048BM96	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4048BMT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4048BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4048BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4048BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

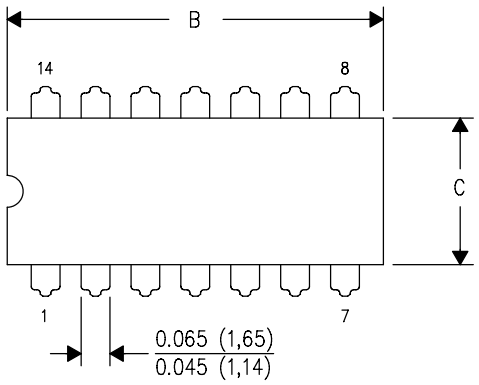
(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

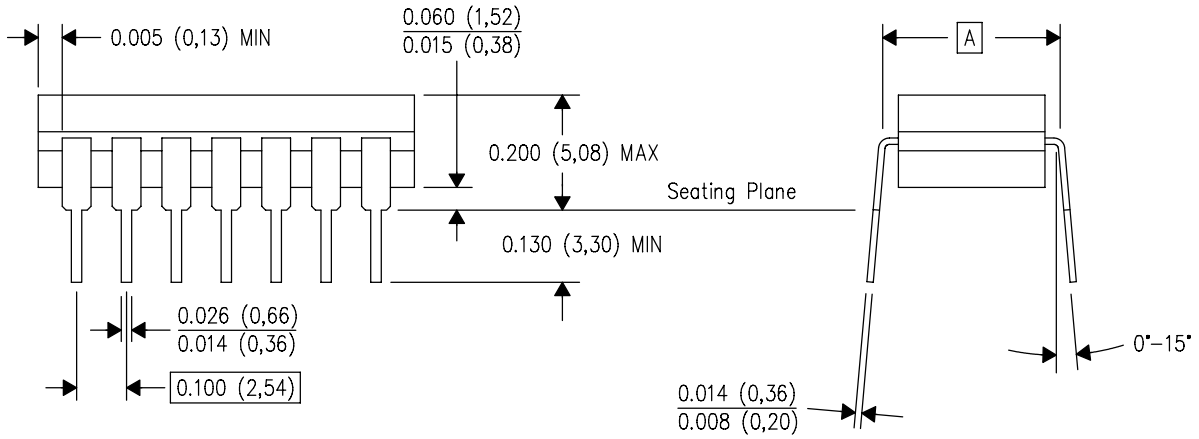
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



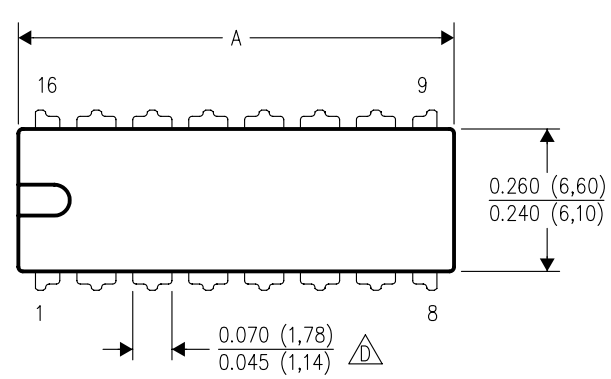
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

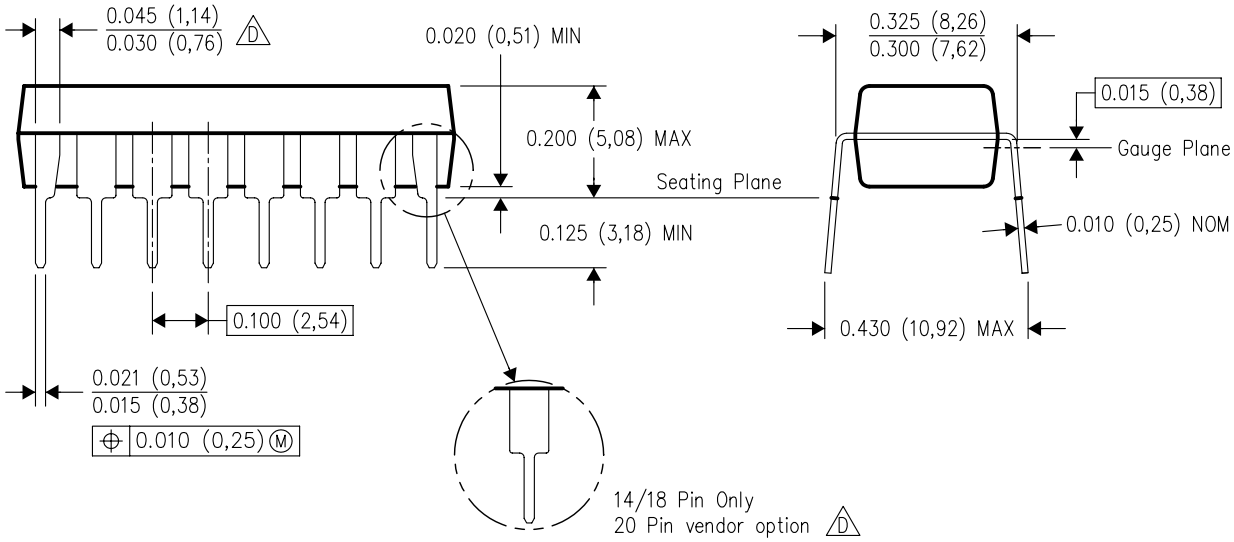
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



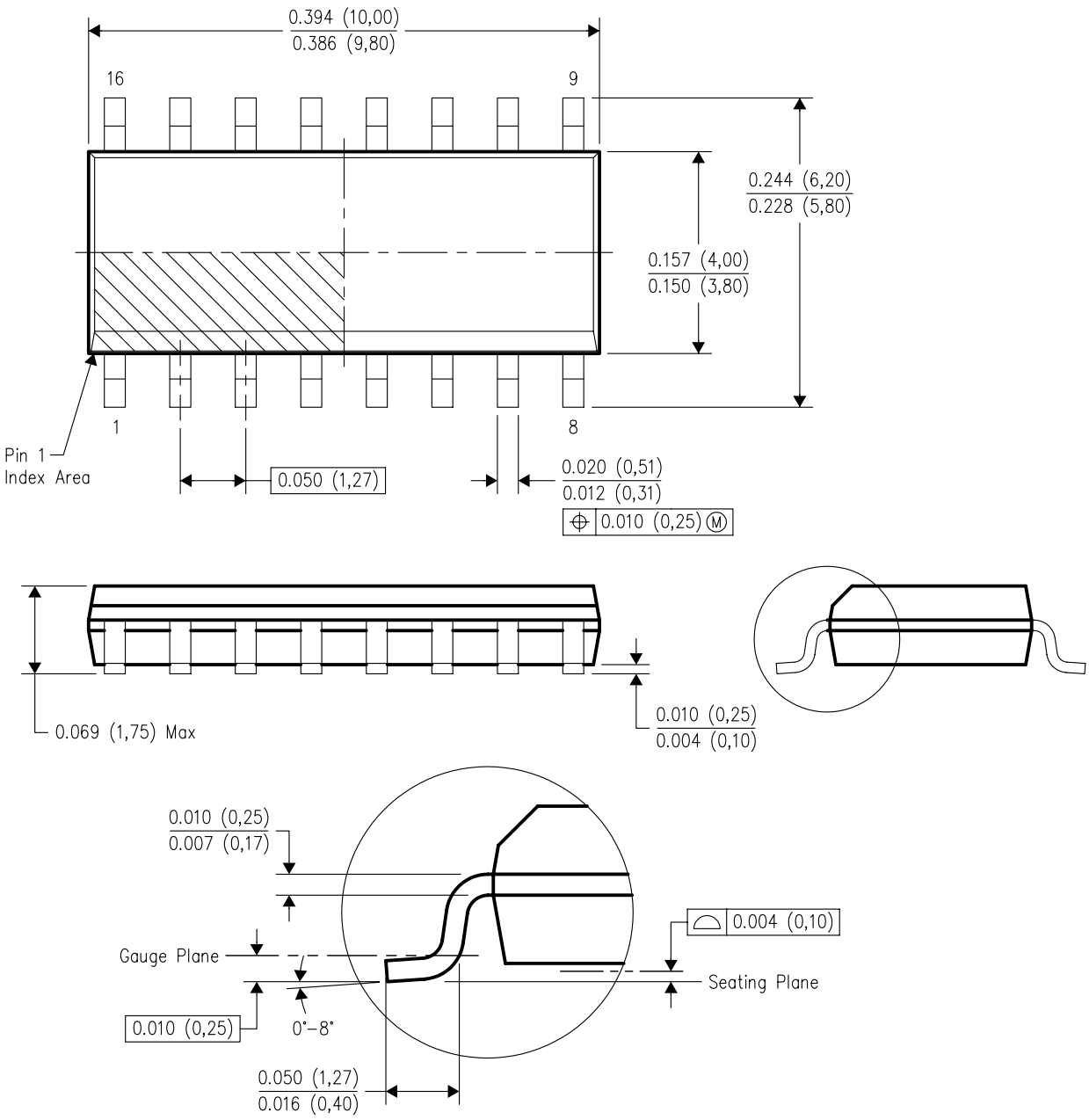
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

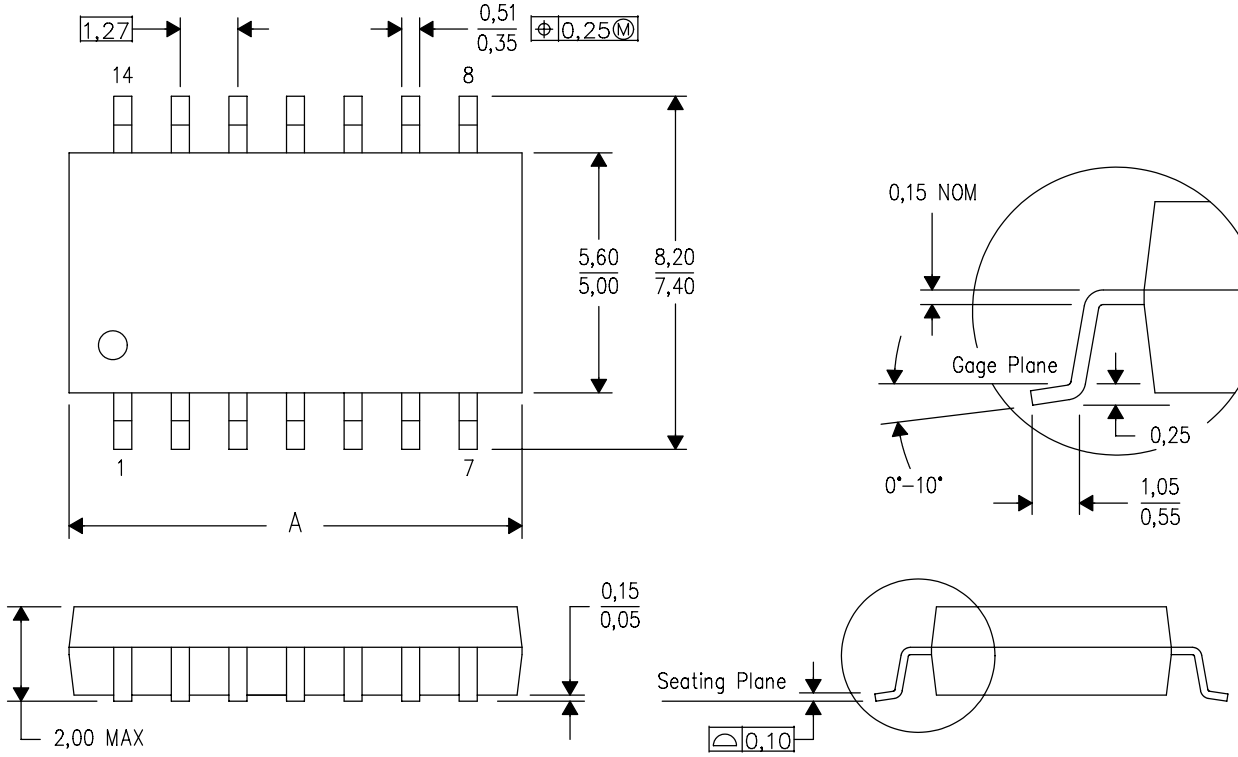


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



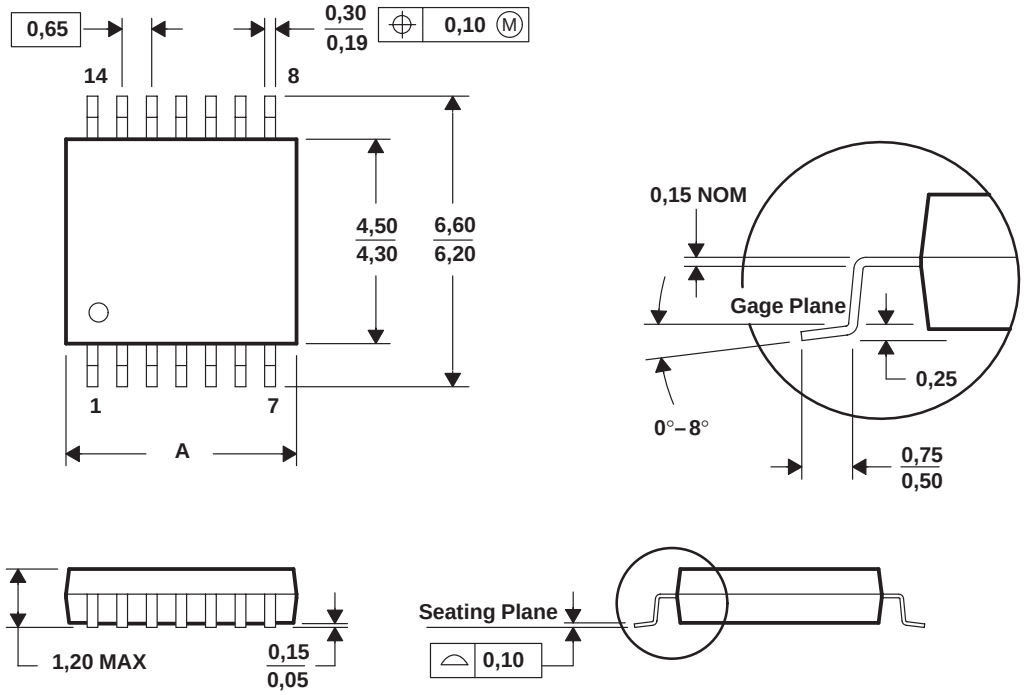
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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